WHAT IS CLAIMED IS:

1. A low noise amplifier, comprising:

a radio frequency input; and

an electrostatic discharge protection circuit including,

a pair of diodes each having a first and a second terminal;

a first diode of the pair having a first terminal coupled to the radio frequency input and a second terminal coupled to a first supply; and

a second diode of the pair having a second terminal coupled to the radio frequency input and a first terminal coupled to the first supply;

the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply.

2. The low noise amplifier of claim 1, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices.

3. The low noise amplifier of claim 1, wherein the first supply is one of a low voltage supply and a high voltage

supply, and

if the first supply is a low voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply,

if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

4. The low noise amplifier of claim 1, further comprising an electrostatic discharge clamp to provide a discharge path between a high voltage supply and a low voltage supply during an electrostatic discharge event.

5. The low noise amplifier of claim 3, wherein the positive and negative electrostatic discharge events include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

6. The low noise amplifier of claim 5, wherein the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio

frequency input to high voltage supply negative discharge pulse.

7. The low noise amplifier of claim 5, wherein the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

8. The low noise amplifier of claim 1, wherein the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

9. A low noise amplifier, comprising:

receiving means for receiving an RF input; and

shunting means including,

a pair of diode means each having a first terminal and a second terminal;

a first diode means of the pair having a first terminal coupled to the receiving means and a second terminal coupled to a first supply; and

a second diode means of the pair having a second terminal coupled to the receiving means and a first

terminal coupled to the first supply;

the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply.

10. The low noise amplifier of claim 9, wherein the shunting means is formed by one of polymer device means and metal oxide silicon device means.

11. The low noise amplifier of claim 9, wherein the first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the shunting means is not directly coupled to a corresponding high voltage supply,

if the first supply means is a high voltage supply, then the shunting means is not directly coupled to a corresponding low voltage supply.

12. The low noise amplifier of claim 9, further comprising clamping means for providing a discharge path between the high voltage supply and the low voltage supply during an

electrostatic discharge event.

13. The low noise amplifier of claim 11, wherein the positive and negative electrostatic discharge events include a receiving means to high voltage supply positive discharge pulse, a receiving means to high voltage supply negative discharge pulse, a receiving means to low voltage supply positive discharge pulse, and a receiving means to low voltage supply negative discharge pulse.

14. The low noise amplifier of claim 13, wherein the low voltage supply floats during the receiving means to high voltage supply positive discharge pulse and the receiving means to high voltage supply negative discharge pulse.

15. The low noise amplifier of claim 13, wherein the high voltage supply floats during the receiving means to low voltage supply positive discharge pulse and the receiving means to low voltage supply negative discharge pulse.

16. The low noise amplifier of claim 9, wherein the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e,

802.11g, 802.11h, and 802.11i, and 802.14.

17. An electrostatic discharge protection circuit, comprising:

a pair of diodes each having a first terminal and a second terminal;

a first diode of the pair having a first terminal coupled to an input/output pad and a second terminal coupled to a first supply; and

a second diode of the pair having a second terminal coupled to the input/output pad and a first terminal coupled to the first supply;

the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events.

18. The circuit of claim 17, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices.

19. The circuit of claim 17, wherein first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the electrostatic discharge protection circuit is not directly

coupled to a corresponding high voltage supply,

if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

20. The circuit of claim 17, further comprising an electrostatic discharge clamp to provide a discharge path between a high voltage supply and a low voltage supply during an electrostatic discharge event.

21. The circuit of claim 19, wherein the positive and negative electrostatic discharge events include an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

22. The circuit of claim 21, wherein the low voltage supply floats during the input/output pad to high voltage supply positive discharge pulse and the input/output pad to high voltage supply negative discharge pulse.

23. The circuit of claim 21, wherein the high voltage supply floats during the input/output pad to low voltage supply positive discharge pulse and the input/output pad to low voltage supply negative discharge pulse.

24. An electrostatic discharge protection circuit for discharging electrostatic discharge events, comprising:

shunting means including,

a pair of diode means having a first terminal and a second terminal;

a first diode means of the pair having a first terminal coupled to an input/output pad and a second terminal coupled to a first supply; and

a second diode means of the pair having a second terminal coupled to the input/output pad and a first terminal coupled to the first supply;

the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.

25. The electrostatic discharge protection circuit of claim 24, wherein the shunting means is formed by one of polymer device means and metal oxide silicon device means.

26. The electrostatic discharge protection circuit of claim 24, wherein the first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the shunting means is not directly coupled to a corresponding high voltage supply,

if the first supply means is a high voltage supply, then the shunting means is not directly coupled to a corresponding low voltage supply.

27. The electrostatic discharge protection circuit of claim 24, further comprising clamping means for providing a discharge path between a high voltage supply and a low voltage supply during an electrostatic discharge event.

28. The electrostatic discharge protection circuit of claim 26, wherein the positive and negative electrostatic discharge events include an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

29. The electrostatic discharge protection circuit of claim 28, wherein the low voltage supply floats during the input/output pad to high voltage supply positive discharge pulse and the input/output pad to high voltage supply negative discharge pulse.

30. The electrostatic discharge protection circuit of claim 28, wherein the high voltage supply floats during the input/output pad to low voltage supply positive discharge pulse and the input/output pad to low voltage supply negative discharge pulse.

31. A method for discharging electrostatic discharge, comprising:

providing a first discharge path between an input/output pad and a first supply;

providing a second discharge path between the input/output pad and the first supply; and

shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path.

32. The method of claim 31, wherein providing a first discharge path and a second discharge path includes providing

a first discharge path and a second discharge path between the input/output pad and one of a low voltage supply and a high voltage supply,

if the first discharge path and the second discharge path are provided between the input/output pad and a low voltage supply, then not providing a direct discharge path between the input/output pad and a corresponding high voltage supply,

if the first discharge path and the second discharge path are provided between the input/output pad and a high voltage supply, then not providing a direct discharge path between the input/output pad and a corresponding low voltage supply.

33. The method of claim 31, further comprising providing a discharge path between the high voltage supply and the low voltage supply during an electrostatic discharge event.

34. The method of claim 32, wherein shunting electrostatic discharge current includes shunting one or more of an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

35. The method of claim 34, wherein shunting an input/output pad to high voltage supply positive discharge pulse and shunting an input/output pad to high voltage supply negative discharge pulse includes floating the low voltage supply.

36. The method of claim 34, wherein shunting an input/output pad to low voltage supply positive discharge pulse and shunting an input/output pad to low voltage supply negative discharge pulse includes floating the high voltage supply.